DEPARTMENT OF ELETRONICS AND COMMUNICATION ENGINEERING
Course Structure for M.Tech (VLSI) w.e f. AY:2020-21

SEMESTER I

Category	Course Title	Contact Periods per week				Credits
		L	T	P	Total	
PC	Analog CMOS IC design	3	0	0	3	3
PC	Digital CMOS IC design	3	0	0	3	3
PE	Professional Elective I	3	0	0	3	3
PE	Professional Elective II	3	0	0	3	3
PC	RTL Simulation and Synthesis with PLDs Lab	0	0	3	3	1.5
PC	CMOS IC Design Lab	0	0	3	3	1.5
HS	Research Methodology and IPR	2	0	0	2	2
HS	Audit Course - I	2	0	0	2	0
SOC	Value Added Course/Certificate Course I	0	0	0	0	1
	Activity Point Programme	During the Semester				25 points
	Total	**16**	**0**	**6**	**22**	**18**

SEMESTER II

Category	Course Title	Contact periods per week				Credits
		L	T	P	Total	
PC	ASIC Design	3	0	0	3	3
PC	Embedded System Design	3	0	0	3	3
PE	Professional Elective III	3	0	0	3	3
PE	Professional Elective IV	3	0	0	3	3
PC	ASIC CAD Lab	0	0	3	3	1.5
PC	Embedded System Design Lab	0	0	3	3	1.5
HS	Audit Course - II	2	0	0	2	0
EEC	Mini Project	0	0	4	4	2
SOC	Value Added Course/Certificate Course II	0	0	0	0	1
	Activity Point Programme	During the Semester				25 points
	Total	**14**	**0**	**10**	**24**	**18**

SEMESTER III

Category	Course Title	Contact Periods per week				Credits
		L	T	P	Total	
PE	Professional Elective V	3	0	0	3	3
OE	Open Elective	3	0	0	3	3
EEC	Teaching Assignment	-	-	-	-	**2**
PRO	Project I	0	0	16	16	**8**
	Activity Point Programme	During the Semester				25 points
	Total	**6**	**0**	**20**	**26**	**16**

SEMESTER IV

Category	Course Title	Contact Periods per week				Credits
		L	T	P	Total	
PRO	Project II	0	0	32	32	16
	Activity Point Programme	During the Semester				25 points
		0	**0**	**32**	**32**	**16**

Professional Electives:

Professional Elective-1	Professional Elective-2	Professional Elective-3	Professional Elective-4	Professional Elective-5
VLSI Signal Processing	Parallel Processing	RF IC Design	Mixed - Signal Circuit Design	Communication Network
Advanced Computer Architecture	CAD of Digital System	Testing and Testability	Internet of Things	Genetic Algorithms and their Applications in VLSI
VLSI Technology	Low Power VLSI Design	CPLD and FPGA Architectures And Applications	Physical Design Automation	Nano Electronics

Open Elective:

Open Elective
1. Business Analytics
2. Industrial Safety
3. Operations Research
4. Cost Management of Engineering Projects
5. Composite Materials
6. Waste to Energy

Audit Courses:

Audit Courses
1. English For Research Paper Writing
2. Sanskrit
3. Disaster Management
4. Value Education
5. Constitution Of India
6. Pedagogical Studies
7. Stress Management By Yoga
8. Personality Development through Life and Enlightenment Skills

S NO	SUBJECT AREA	Credits per semester				Credits
		I	II	III	IV	
1	HS	2	-	-	-	**2**
2	PC	9	9		-	**20**
3	PE	6	6	3	-	**15**
4	OE	-	-	3	-	**3**
5	PRO	-	-	8	16	**26**
6	SOC	1	1	-	-	**2**
7	EEC	-	2	2	-	**2**
TOTAL		**18**	**18**	**16**	**16**	**68**

DEPARTMENT OF ECE

List of Subjects approved by BoS of ECE Department held on 09.01.2021 for M.Tech (VLSI)

S. No	Subjects	Sem	Category
1	Analog CMOS IC Design	I Sem	PC
2	Digital CMOS IC Design	I Sem	PC
3	RTL Simulation and Synthesis with PLDs lab	I Sem	PC
4	CMOS IC Design Lab	I Sem	PC
5	ASIC Design	II Sem	PC
6	Embedded System Design	II Sem	PC
7	ASIC CAD Lab	II Sem	PC
8	Embedded System Design Lab	II Sem	PC
9	VLSI Signal Processing	I Sem	PE 1
10	Advanced Computer Architecture	I Sem	PE 1
11	VLSI Technology	I Sem	PE 1
12	Parallel Processing	I Sem	PE 2
13	CAD of Digital System	I Sem	PE 2
14	Physical Design Automation	I Sem	PE 2
15	RF IC Design	II Sem	PE 3
16	Testing and Testability	II Sem	PE 3
17	CPLD and FPGA Architectures and Applications	II Sem	PE 3
18	Mixed - Signal Circuit Design	II Sem	PE 4
19	Internet of Things	II Sem	PE 4
20	Low Power VLSI Design	II Sem	PE 4
21	Communication Networks	III Sem	PE 5
22	Genetic Algorithms and their Applications in VLSI	III Sem	PE 5
23	Nano Electronics	III Sem	PE 5

1. ANALOG CMOS IC DESIGN

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
I	3	0	0	48	3	40	60	100

MODULE – 1 MOS DEVICES AND MODELING 9 h

The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

MODULE -2 ANALOG CMOS SUB-CIRCUITS 7 h

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage Reference, Band gap Reference.

MODULE-3 CMOS AMPLIFIERS 8 h

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures, Mismatch-offset cancellation techniques, Reduction of Noise by offset cancellation techniques, Alternative definition of CMRR.

MODULE-4 CMOS OPERATIONAL AMPLIFIERS 8 h

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

MODULE-5 COMPARATORS 10 h

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators

MODULE-6 SWITCHED CAPACITOR CIRCUITS 7 h

General Considerations - Sampling Switches - MOSFETS as Switches - Speed Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers - Unity-Gain Sampler/Buffer, Noninverting Amplifier, Precision Multiply-by-Two Circuit.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.
2. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce,
3. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

2. DIGITAL CMOS IC DESIGN

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
I	3	0	0	48	3	40	60	100

MODULE – 1 INTRODUCTION TO DIGITAL DESIGN 8 h

Building Blocks For Digital Design: Multiplexer, Demultiplexer, Decoder, Encoder, Comparator, Adder, ALU, Carry-look-ahead adder.Building Blocks With Memory: Clocked building blocks, register building blocks, RAM,ROM, PLA, PAL, Timing devices.Study RAM,ROM,PLA,PAL and alloyed solid state memories.

MODULE -2 ASM DESIGN 8 h

DESIGN METHODS: Elements of design style, top-down design, separation of controller and architecture, refining architecture, and control algorithm, Algorithmic State Machines, ASM chart notations. Realising ASMS - Traditional synthesis from ASM chart, multiplexer controller method, one-hot method, ROM based method. Asynchronous Inputs And Races - Asynchronous ASMs, Design for testability, test vectors, fault analysis tools.

MODULE-3 MOS DESIGN PSEUDO NMOS LOGIC 8 h

Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

MODULE-4 COMBINATIONAL MOS LOGIC CIRCUITS 10 h

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

MODULE-5 SEQUENTIAL MOS LOGIC CIRCUITS 7 h

Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

MODULE-6 MODELLING WITH VHDL 7 h

CAD tools, simulators, schematic entry, synthesis from VHDL. Design Case Studies: Single pulse, system clock, serial to parallel data conversion, traffic light controller.

Text Book(s):

1. Digital System Design using VHDL-Roth, Mc. Graw Hill,2000.
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3RD eD., 2011.

Reference Book(s):

1. An Engineering Approach to Digital Design -William Fletcher, 1st Edition, Prentice- Hall India1997.
2. Digital Systems Engineering -William J Dally and John W Poulton, Cambridge University Press, 2008.
3. A VHDL Primer -Jayaram Bhasker, 3rd edition, Prentice-Hall India,2009.
4. VHDL for Programmable Logic -Kevin Skahill, CypressSemiconductors.
5. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
6. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan, BorivojeNikolic, 2nd Ed., PHI.
7. Franklin P. Prosser and David E. Winkel, "The Art of Digital Design", PrenticeHall

3. RTL SIMULATION AND SYNTHESIS WITH PLDS LAB

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
I	0	0	3	48	1.5	40	60	100

Task 1 –HDL implementation of Multiplexrs and Demultiplexers

Objectives: To implement 8:1 MUX/De-MUX using HDL

Task 2–HDL implementation of3-bit Synchronous Counters

Objectives: To implement 3-bit Synchronous counters using HDL

Task 3–HDL implementation of Comparator and Parity Generator

Objectives: To implement 8-bit Magnitude Comparator HDL

d) To implement Parity Generator HDL

Task 4–HDL implementation of Encoder and Decoder

Objectives: To implement Encoder/decoder using VHDL

Task 5-Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.

Objectives: a) To implement sequence generators/detectors

b) To implement Synchronous FSM

To implement Mealy and Moore machines.

Task 6-HDL implementation **of** Traffic Light controller,

Objectives: To design Traffic light controller using HDL

Task 7-HDL implementation of Vending machine

Objectives: To design Vending machines using HDL

Task 8-HDL implementation of ATM,

Objectives: To design ATM using HDL

Task 9-UART/ USART implementation in HDL.

Objectives: a) To implement UART/ USART

Task 10 - Realization of single port SRAM in HDL

Objectives: To determine the performance characteristics

Task 11–HDL implementation of Arithmetic circuits like serial adder/ Subtractor, parallel adder/Subtractor, serial/parallel multiplier.

Objectives:.To design arithmetic circuits using HDL

Task 12- Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

Objectives: To implement the FFT algorithm using verilog.

Text Book(s):

1. Modern Digital Design -Richard S. Sandige, MGH, International Editions.
2. Digital principles and Design -Donald D Givone, TMH.
3. Charles Roth, Jr. and Lizy K John, "Digital System Design using VHDL", Cengage Learning.

Reference Book(s):

1. Verilog HDL, a guide to digital design and synthesis-Samir Palnitkar, Prentice Hall.
2. FPGA based prototyping methodology manual -Doug Amos, Austin Lesea, Rene Richter, Xilinx.
3. Designing with FPGAs & CPLDs -Bob Zeidman, CMP Books

4. CMOS IC DESIGN LAB

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
I	0	0	3	48	1.5	40	60	100

Task 1: MOS Device Characterization and parametric analysis

Objective: Design and implement the Layout of MOS Device using CMOS Technology with Mentor Graphics Tool

Task 2: Common Source Amplifier

Objective: Design and implement the Layout of Common Source Amplifier using CMOS Technology with Mentor Graphics Tool

Task 3: Common Source Amplifier with source degeneration

Objective: Design and implement the Layout of Common Source Amplifier with source degeneration using CMOS Technology with Mentor Graphics Tool

Task 4: Cascode amplifier

Objective: Design and implement the Layout of Cascode amplifier using CMOS Technology with Mentor Graphics Tool

Task 5: simple current mirror

Objective: Design and implement the Layout of simple current mirror using CMOS Technology with Mentor Graphics Tool

Task 6: cascode current mirror.

Objective: Design and implement the Layout of cascode current mirror.using CMOS Technology with Mentor Graphics Tool

Task 7: Wilson current mirror.

Objective: Design and implement the Layout of Wilson current mirror. using CMOS Technology with Mentor Graphics Tool

Task 8: Full Adder

Objective: Design and implement the Layout of Full Adder using CMOS Technology with Mentor Graphics Tool

Task 9: RS-Latch

Objective: Design and implement the Layout of RS- latch using CMOS Technology with Mentor Graphics Tool

Task 10: Clock Divider

Objective: Design and implement the Layout of using Clock Divider CMOS Technology with Mentor Graphics Tool

Task 11: JK-Flip Flop

Objective: Design and implement the Layout of JK-Flip Flop using CMOS Technology with Mentor Graphics Tool

Task 12: Synchronous Counter

Objective: Design and implement the Layout using CMOS Technology with Mentor Graphics Tool

Text Book(s):

1. Modern Digital Design -Richard S. Sandige, MGH, International Editions.
2. Digital principles and Design -Donald D Givone, TMH.
3. Digital System Design using VHDL -Charles Roth, Jr. and Lizy K John, Cengage Learning.

Reference Book(s):

1. Verilog HDL, a guide to digital design and synthesis -Samir Palnitkar, Prentice Hall.
2. Designing with FPGAs & CPLDs -Bob Zeidman, CMP Books

5. ASIC DESIGN

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
II	3	0	0	48	3	40	60	100

MODULE – 1 INTRODUCTION TO ASICs 8 h

Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

MODULE -2 PROGRAMABLE ASICS AND PROGRAMABLE ASIC LOGIC CELLS 8 h

The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

MODULE-3 I/O CELLS AND INTERCONNECTS & SOFTWARE 8 h

DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

MODULE-4 LOW LEVEL DESIGN ENTRY AND LOGIC SYNTHESIS 8 h

Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

MODULE-5 SIMULATION 8 h

Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation.

MODULE-6 TEST AND ASIC CONSTRUCTION 8 h

The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods.

Text Book(s):

1. Application Specific Integrated Circuits -Michael John Sebastian Smith, Pearson Education, 2003.

2. Integrated Circuit Engineering -L.J. Herbst, Oxford Science Publications, 1996.

Reference Book(s):

1. Advanced ASIC Chip Synthesis using Synopsis Design compiler -Himanshu Bhatnagar, 2nd Edition, Kluwer Academic, 2001

6. EMBEDDED SYSTEM DESIGN

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
II	3	0	0	48	3	40	60	100

MODULE – 1 INTRODUCTION TO EMBEDDED SYSTEMS 8 h

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

MODULE -2 TYPICAL EMBEDDED SYSTEM 10 h

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

MODULE-3 EMBEDDED FIRMWARE 8 h

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

MODULE-4 RTOS BASED EMBEDDED SYSTEM DESIGN 7 h

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

MODULE-5 TASK COMMUNICATION 8 h

Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

MODULE-6 DESIGN EXAMPLES 7 h

Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes.

Text Book(s):

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.
2. Embedded Systems - Raj Kamal,TMH.
3. Computers as a component: principles of embedded computing system design- wayne wolf.

Reference Book(s):

1. Embedded System Design - Frank Vahid, Tony Givargis, JohnWiley.
2. Embedded Systems – Lyla, Pearson,2013
3. An Embedded Software Primer - David E. Simon, PearsonEducation

7. ASIC CAD Lab

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
II	0	0	3	48	1.5	40	60	100

Task 1 : Mixed signal simulation.
Objective : Design and simulate mixed-signal application based circuits o (circuits consisting of both analog and digital parts)Mentor Graphic Tool

Task 2: Layout Extraction.
Objective : To extract Layout from Digital Circuits using Mentor Graphics.

Task 3: Critical Path Estimation
Objective : To verify timing simulation for critical path time calculation

Task 4 : Parasitic values estimation from layout
Objective : To determine parasitic values from Layout using Mentor Graphics tool

Task 5: Layout Vs Schematic
Objective : To study the layout vs schematic for Digital circuits

Task 6: Net List Extraction.
Objective : To Extract the netlist of NAND gate

Task 7: Design Rule Checks.
Objective : To verify the design rules of layout using DRC

Task 8: Floor Planning
Objective : To study the Floor Planning in digital circuit

Task 9: Routing and Placement Procedure
Objective : To study the Route and Place Procedure in digital circuit

Task 10: Power estimation
Objective : To study the Power Estimation in digital circuit

Text Book(s):
1. Application Specific Integrated Circuits -Michael John Sebastian Smith, Pearson Education, 2003.
2. Integrated Circuit Engineering -L.J.Herbst, Oxford Science Publications, 1996.

Reference Book(s):
1) Advanced ASIC Chip Synthesis using Synopsis Design compiler -HimanshuBhatnagar, 2nd Edition, Kluwer Academic, 2001.

8. EMBEDDED SYSTEM DESIGN LABORATORY

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
II	0	0	3	48	1.5	40	60	100

Task-1: Basic Embedded C Programs**.**

Objectives: a) Write a simple program to print "hello world"

b) Write a simple program to show a delay.

Task-2: Testing of Hardware timeout Loops

Objective: Write a c program to test hardware based timeout loops.

Task-3: Traffic light Sequencing

Objectives: Develop a simple EOS showing traffic light sequencing

Task-4: Elapsed Time Display

Objective: Write a program to display elapsed time over RS-232 link.

Task-5: Milk Pasteurization system

Objective: Develop software for milk Pasteurization system.

Task-6: Study of Code Composer Studio

Objective: A Study of Code Composer Studio (CC Studio Latest Version)

Task-7: Flashing a light

Objective: Flashing a light by a software delay.

Task-8: Display Characters on LCD

Objectives: To Display Characters on LCD.

Task-9: UART Serial communication

Objective: Objectives: Serial Communication Using UART.

Task-10: MSP430 UART

Objective: Objectives: Basic Input and Output Using MSP430 UART

Task-11: Interrupt handling

Objectives: Interrupt handling Using MSP430

Task-12: ADC Using MSP430

Objectives: Analog to Digital Conversion Using MSP430

Additional Experiments:

TASK-13: verification of SEOS Timer

Objective: Write a program to drive SEOS using Timer 0.

TASK-14: GPIO Ports

Objective: Interfacing external Devices to GPIO Ports

Text Book (s):

1. Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers -Tammy Noergaard, Elsevier(Singapore) Pvt.Ltd.Publications, 2005.

2. MSP430 Microcontroller Basics -John H. Davies, Elsevier Ltd Publications, Copyright 2008.

Reference Book(s):

1. Introduction to Embedded Systems Using Microcontrollers and the MSP430-Manuel Jiménez Rogelio, PalomeraIsidoroCouvertier, Springer Publications, 2014.

2. Embedded system Design: A Unified Hardware/Software Introduction-Frank Vahid, Tony D. Givargis, John Wily & Sons Inc.2002.

3. Embedded System Design-Peter Marwedel, Science Publishers, 2007.

4. Embedded System Design -Arnold S Burger, CMP Books, 2002.

5. Embedded Systems: Architecture, Programming and Design-Rajkamal, TMH Publications, Second Edition, 2008.

9. VLSI SIGNAL PROCESSING

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
I	3	0	0	48	3	40	60	100

MODULE-1 Introduction to Digital Signal Processing Systems 8 h

Introduction to Digital Signal Processing Systems: Introduction, Typical DSP Algorithms, Representations of DSP Algorithms.

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power.

Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.

MODULE-2 Unfolding and Folding 8 h

Unfolding: Introduction, Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming, Applications of Unfolding. **Folding:** Introduction, Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.

MODULE-3 Bit level arithmetic structures 8h

Bit level arithmetic structures- parallel multipliers, interleaved floor plan and bit plan based digital filters, Bit serial multipliers. Bit serial filter design and implementation,Canonic signed digit arithmetic, Distributed arithmetic.

MODULE-4 Redundant arithmetic 9h

Redundant arithmetic, redundant number representations carry free radix 2 addition and subtraction, Hybrid radix 4 addition, Radix 2 hybrid redundant multiplication architectures, data format conversion, Redundant to no redundant converter.

NUMERICAL SRENGTH REDUCTION: Introduction, Sub expression Elimination, Multiple constant multiplications, Sub expression sharing in digital filters, additive and multiplicative number splitting.

MODULE-5 Synchronous, Wave, Asynchronous Pipelines 8h

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining, Implementation of wave-pipelined systems. Asynchronous pipelining.

MODULE-6 Low Power Design 7h

Scaling versus power consumption, Power analysis, power reduction techniques, power estimation techniques, Low power IIR filter design, Low power CMOS lattice IIR filter.

Text Book(s):

1. VLSI Digital Signal Processing systems, John Wiley -K.K. Parhi, 1999.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

Reference Book(s):

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

10. ADVANCED COMPUTER ARCHITECTURE

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
I	3	0	0	48	3	40	60	100

MODULE-1 PARALLEL COMPUTER MODELS 8 h

System attributes to performance, Multiprocessors and Multicomputers, Classifications of Architectures, Multivector and SIMD Computers, Architecture development tracks

MODULE-2 PROGRAM AND NETWORK PROPERTIES 9 h

Conditions for parallelism, Program partitioning and Scheduling, Program flow mechanisms, System interconnect architectures, Performance metrics and measures, Parallel Processing Applications

MODULE-3 PROCESSORS AND MEMORY HIERARCHY 8 h

Advanced Processor Technology, Superscalar and Vector processors, Memory hierarchy technology, Virtual Memory, Backplane bus systems, Cache memory organizations, Shared memory organizations
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MODULE-4 PIPELINES 8 h

Pipelining and Superscalar Techniques Linear Pipeline processors, Nonlinear pipeline processors, Instruction pipeline design, Arithmetic pipeline design, Superscalar and Super Pipeline Design

MODULE-5 MULTIPROCESSORS AND MULTI-COMPUTERS 8 h

Multiprocessor System Interconnects, Cache Coherence and Synchronization mechanisms, Three generations of Multicomputers, Message passing mechanisms, Vector Processing principles, Principles of Multithreading

MODULE-6 THREAD LEVEL PARALLELISM 7 h

Thread level Parallelism Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

TEXT BOOK(S):

1. Advanced Computer Architecture-Hwang kai, McGraw-Hill, 2001.
2. Computer Architecture-Patterson, Morgn Kaufmann, 2001.
3. Computer Architecture: A Quantitative Approach-John L. Hennessy, David A. Patterson, 3rd Edition, An Imprint of Elsevier.

REFERENCE BOOK(S):

1. Computer Organization and Architecture-William Stallings, 8th Edition, Prentice-Hall India, 2010.
2. Computer Organization and Design-D. A Patterson and J. L. Hennesey, 4th Ed., Elsevier India, 2011.
3. Structured Computer Organization-Andrew S Tanenbaum and James R Goodman, 5th Edition Prentice Hall India, 2009.

11. VLSI TECHNOLOGY

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
I	3	0	0	48	3	40	60	100

MODULE-1 Review of Microelectronics and Introduction to MOS Technologies 8 h

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS &BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

MODULE-2 MOS STRUCTURES 7 h

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

MODULE-3 COMBINATIONAL LOGIC NETWORKS 10 h

Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing

MODULE-4 SEQUENTIAL SYSTEMS 7 h

Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing

MODULE-5 FLOOR PLANNING & ARCHITECTURE DESIGN 7 h

Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

MODULE-6 INTRODUCTION TO CAD SYSTEMS AND CHIP DESIGN 9 h

LayoutSynthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

Text Book(s):

1. Essentials of VLSI Circuits and Systems, K. Eshraghianet . al(3 authors) PHI of India Ltd.,2005
2. Modern VLSI Design, 3rd Edition, Wayne Wolf , Pearson Education, fifth Indian Reprint, 2005.
3. VLSI Design-P.P. Sahu, TMH, 1st edition 2013.

Reference Book(s):

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.
3. CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.

12. PARALLEL PROCESSING

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
I	3	0	0	48	3	40	60	100

MODULE – 1 OVERVIEW OF PARALLEL PROCESSING 8 h

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability, Basic Techniques, Parallel Computers for increase Computation speed, Principles and Implementation of Pipelining, Classification of pipelining processors.

MODULE -2 PARALLEL COMPUTING 8 h

Parallel Computers for increase Computation speed, Parallel & Cluster Computing, Advanced pipelining techniques, Software pipelining.

MODULE-3 VLIW PROCESSORS & MESSAGE PASSING 8 h

VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, Message Passing Technique- Evaluating Parallel programs and debugging, Portioning and Divide and Conquer strategies examples

MODULE-4 MULTITHREADED SYSTEMS 8 h

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

MODULE-5 PARALLEL PROGRAMMING TECHNIQUES 8 h

Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Pipelining- Techniques computing platform, pipeline programs examples

MODULE-6 MULTIPROCESSORS SYSTEMS 8 h

Operating systems for multiprocessors systems, customizing applications on parallel processing platforms**.**

Text Book(s):

1. Parallel Programming, Barry Wilkinson, Michael Allen, Pearson Education, 2nd Edition.
2. Parallel Computers -V. Rajaraman, L. Sivaram Murthy, PHI.
3. Introduction to Parallel algorithms by Jaja from Pearson, 1992.

Reference Book(s):

1. Computer Architecture and Parallel Processing -Kai Hwang, Faye A. Briggs, MGH International Edition
2. Advanced Computer Architecture-Kai Hwang, TMH
3. Computer Organization and Architecture, Designing for performance-William Stallings, Prentice Hall, Sixth edition
4. Scalable Parallel Computing-Kai Hwang, Zhiwei Xu, MGH
5. Digital Design and Computer Architecture-David Harris and Sarah Harris, Morgan Kaufmann.

13. CAD OF DIGITAL SYSTEM

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
I	3	0	0	48	3	40	60	100

MODULE – 1 VLSI PHYSICAL DESIGN AUTOMATION 8 h

VLSI Physical Design Automation VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

MODULE -2 PARTITIONING 8 h

Partitioning– Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.

MODULE-3 FLOOR PLANNING , PIN ASSIGNMENT AND PLACEMENT 8 h

Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms. Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

MODULE-4 GLOBAL ROUTING& DETAILED ROUTING 8 h

Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

MODULE-5 PHYSICAL DESIGN AUTOMATION OF FPGAS AND MCMS 8 h

Physical Design Automation of FPGAs and MCMs FPGA Technologies, Physical Designcycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model ;Introduction to MCM Technologies, MCMPhysical
Design Cycle.

MODULE-6 CHIP INPUT AND OUTPUT CIRCUITS 8 h

Chip input and output circuits :ESD protection, input circuits, Output circuits, on chip clock generation and prevention ,Latch up and its prevention.

Text Book(s):

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang,Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Book(s):

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S.H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

14. PHYSICAL DESIGN AUTOMATION

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
II	3	0	0	48	3	40	60	100

MODULE – 1 INTRODUCTION: LAYOUT AND DESIGN RULES 8 h

Introduction: Layout and design rules, materials for VLSI fabrication, basic algorithmic concepts for physical design, physical design processes and complexities. Partition: Kernigham-Lin's algorithm, Fiduccia Mattheyes algorithm, Krishnamurthy extension, hMETIS algorithm, multilevel partition techniques

MODULE -2 FLOOR-PLANNING 8 h

Hierarchical design, Wire length estimation, Slicing and non-slicing floor plan, polar graph representation, operator concept, Stockmeyer algorithm for floor planning, mixed integer linear program.

MODULE-3 PLACEMENT: DESIGN TYPES 8 h

ASICs, SoC, Microprocessor RLM; Placement techniques: Simulated annealing, Partition based, analytical, and Hall's quadratic; Timing and congestion considerations.

MODULE-4 ROUTING 8 h

Detailed, global and specialized routing, channel ordering, channel routing problems and constraint graphs, routing algorithms, Yoshimura and Kuh's method, zone scanning and net merging, boundary terminal problem, minimum density spanning forest problem, topological routing, cluster graph representation.

MODULE-5 SEQUENTIAL LOGIC OPTIMIZATION AND CELL BINDING 8 h

Sequential Logic Optimization and Cell Binding: State based optimization, state minimization, algorithms; Library binding and its algorithms, concurrent binding

MODULE-6 PERFORMANCE ISSUES IN CIRCUIT LAYOUT 8 h

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing - Driven Placement: Zero Stack Algorithm- Weight based placement - Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem - Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization.

Text Book(s):

1. An Introduction to VLSI Physical Design-Sarrafzadeh, M. and Wong, C.K, 4th Edition, Mc Graw-Hill
2. Modern VLSI Design System on Silicon-Wolf. W, 2nd Ed., Pearson Education.
3. Evolutionary Algorithms for VLSI CAD-Dreschler, 3rd Edition, Springer.

Reference Book(s):

1. VLSI Physical Design Automation: Theory and Practice-Sait, S.M, and Youssef, 1999, World Scientific Publishing Company.
2. Algorithms for VLSI Physical Design Automation-Sherwani, 2nd Edition, Kluwer.
3. Practical Problems in VLSI Physical Design Automation -Lim, S.K, Springer

15. RF IC DESIGN

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
II	3	0	0	48	3	40	60	100

MODULE 1 BASIC CONCEPTS IN RF DESIGN 8 h

Introduction to RF Design, Units in RF design, Time Variance and Nonlinearity, Effects of nonlinearity, random processes and Noise, Definitions of sensitivity and dynamic range, Passive impedance transformation, Scattering parameters.

MODULE 2 TRANSCEIVER ARCHITECTURES 8 h

General considerations, Receiver Architectures-Basic Heterodyne receivers, Modern heterodyne receivers, Direct conversion receivers, Image-Reject receivers, Low-IF receivers. Transmitter Architectures-Direct Conversion transmitters, Modern direct conversion Transmitters, Heterodyne Transmitters, Other TransmitterArchitectures.

MODULE 3 LNA AND MIXERS 8 h

General considerations, Problem of input matching, Low Noise Amplifiers design in various topologies, Gain Switching, Band Switching, Mixers-General considerations, Passive down conversion mixers, Active down conversion mixers, Up conversionmixers.

MODULE 4 OSCILLATORS 8 h

Performance parameters, Basic principles, Cross coupled oscillator, Three point oscillators, Voltage Controlled Oscillators, LC VCOs with wide tuning range, phase noise, Mathematical model of VCOS, Quadrature Oscillators.

MODULE 5 PLL 8 h

PLLS-Phase detector, Type-I PLLs, Type-II PLLs, PFD/CP Nonidealities, Phase noise in PLLs, Loop Bandwidth.

MODULE 6 POWER AMPLIFIER 8 h

Power Amplifiers-General considerations, Classification of power amplifiers, High- Efficiency power amplifiers, Cascode output stages, Large signal impedance matching, Linearization techniques.

Text Books:

1. RF Microelectronics -B.Razavi, Prentice-Hall PTR, 2nd Edition,1998.

Reference Books:

1. The Design of CMOS Radio-Frequency Integrated Circuits-T.H.Lee, Cambridge University Press, 2nd,1998.
2. CMOSCircuitDesign,LayoutandSimulation-R.JacobBaker,HarryW.Li,D.E.Boyce, Prentice- Hall of India,1998.

16. TESTING AND TESTABILITY

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
II	3	0	0	48	3	40	60	100

MODULE – 1 INTRODUCTION TO TESTING 9 h

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

MODULE -2 LOGIC AND FAULT SIMULATION 7 h

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

MODULE-3 CMOS TESTING 8 h

Testing of static and dynamic circuits. Fault diagnosis: Fault models for diagnosis, Cause- effect diagnosis, Effect-cause diagnosis.

MODULE-4 TESTABILITY MEASURES 7 h

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

MODULE-5 BUILT-IN SELF-TEST 10 h

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

MODULE-6 BOUNDARY SCAN STANDARD 7 H

System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Text Book(s):

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits-M.L. Bushnell, V. D. Agrawal, Kluwer Academic Publishers.
2.VLSI Test Principles and Architectures: Design for Testability (The Morgan Kaufmann Series In Systems On Silicon) Hardcover – Import, 14 August 2006)by Laung-Terng Wang.
3."Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", by M. L. Bushnell and V. D. Agrawal,Nov 16, 2015.

Reference Book(s):

1. Digital Systems and Testable Design-M. Abramovici, M. A. Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability-P.K. Lala, Academic Press.

3.“Testing of Digital Systems” by N. K. Jha and S. Gupta.
4. “Built-in Test for VLSI: Pseudorandom Techniques” by P H Bardell and J Savir

17. CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
II	3	0	0	48	3	40	60	100

MODULE – 1 INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES 7h
Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic;

MODULE –2 COMPLEX PROGRAMMABLE LOGIC DEVICES 7h
Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

MODULE-3 FIELD PROGRAMMABLE GATE ARRAYS 9h
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

MODULE – 4 SRAM PROGRAMMABLE FPGAS 8h
Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

MODULE-5 ANTI-FUSE PROGRAMMED FPGAS 8h
Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3 Architectures.

MODULE-6 DESIGN APPLICATIONS 9h
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books:
1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.

Reference Books:
1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier,Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

18. MIXED - SIGNAL CIRCUIT DESIGN

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
II	3	0	0	48	3	40	60	100

MODULE – 1 CMOS& CASCODED STAGES 8 h

CMOS Amplifiers- Common Source with diode connected loads and current source load, CS stage with source degeneration, CG stage and Source Follower (Only Voltage Gain and Output impedance of circuits. **Cascoded stages -** Cascoded amplifier, Cascoded amplifier with cascoded loads , Folded cascode Amplifier

MODULE -2 MOS CURRENT MIRROR& DIFFERENTIAL AMPLIFIERS 8 h

MOS Current Mirror- Basic circuit, PMOS and NMOS current mirrors Current mirror copying circuits, MOSFET cascode current mirror circuits

Differential Amplifiers-Differential Amplifier with MOS current source Load, with cascaded load and with current mirror load, MOS telescopic cascode amplifier. (Only Voltage Gain and Output impedance of circuits

MODULE-3 CMOS OP AMPS& COMPARATOR 8 h

CMOS OP AMPS- Two Stage Operational Amplifiers - Frequency compensation of OPAMPS - miller compensation **,** Design of classical Two Stage OP AMP

Comparator-Characterization of a comparator-static and dynamic, A Two stage open loop comparator (analysis not required)

MODULE-4 BAND GAP REFERENCES & PLL 8 h

Band gap References- Supply Independent Biasing, Temperature independent references –band gap reference

Phase Locked Loop – Simple PLL ,Basic PLL Topology, Charge Pump PLL, Basic Charge Pump PLL**.**

MODULE-5 DYNAMIC ANALOG & SWITCHED CAPACITOR CIRCUITS 8 h

Dynamic analog circuits – charge injection and capacitive feed through in MOS switch, Reduction technique

Switched Capacitor Circuits- sample and hold circuits, Switched Capacitor Integrator, Switched Capacitor Integrator

MODULE-6 DATA CONVERTERS& DAC, ADC ARCHITECTURE 8 h

Data Converters - DAC Specifications-DNL, INL, latency, SNR, Dynamic Range ADC Specifications-Quantization error, Aliasing, SNR, Aperture error.

DAC Architecture - Resistor String, Charge Scaling and Pipeline types.

ADC Architecture- Flash and Pipe line types.

Text Book(s):

1. CMOS Analog Circuit Design-Phillip E. Allen, Douglas R. Holbery, Oxford,2004.
2. Fundamentals of Microelectronics-Razavi B., Wiley studentEdition2014.

Reference Book(s):

1. CMOS: Circuits Design, Layout and Simulation-Baker, Li, Boyce, Prentice HallIndia, 2000.
2. Design of Analog CMOS Integrated Circuits-Razavi B, Mc Graw Hill,2001.

19. INTERNET OF THINGS

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
II	3	0	0	48	3	40	60	100

MODULE 1 FUNDAMENTALS OF IoT 9 h

Evolution of Internet of Things, Enabling Technologies, IoT Architectures,oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects

MODULE -2 NETWORKS AND COMMUNICATION 7 h

Networking Technology, Communication Technology, Processes Data Management, Prototyping embedded devices, Sensors and actuators, Embedded computing basics, Introduction to ARDUINO, RASPBERRY PI

MODULE 3 IoT PROTOCOLS 8 h

IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

MODULE4 DESIGN AND DEVELOPMENT 8 h

Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

MODULE 5 DATA ANALYTICS AND SUPPORTING SERVICES 7 h

Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG

MODULE 6 CASE STUDIES/INDUSTRIAL APPLICATIONS 8 h

IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino)

Text Book(s):

1. Internet of Things: A Hands-on-Approach-Arshdeep Bahga, Vijay Madisetti, VPT, 1st Edition, 2014.
2. Internet of Things: Converging Technologies for Smart
3. Environments and Integrated Ecosystems-Ovidiu Vermesan ,Peter Friess, 2013 River Publishers
4. Internet of Things-Raj Kamal, First edition, McGraw Hill

Reference Book(s):

1. Internet of Things – A hands-on approach, ArshdeepBahga, Vijay Madisetti, Universities Press,2015
2. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit2).
3. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence",Jan Ho¨ ller, VlasiosTsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.

20. LOW POWER VLSI DESIGN

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
II	3	0	0	48	3	40	60	100

MODULE – 1 TECHNOLOGY & CIRCUIT DESIGN LEVELS 8 h

Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamicdissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistorsizing & optimal gate oxide thickness, impact of technology scaling, technologyinnovations

MODULE -2 LOW POWER CIRCUIT TECHNIQUES 8 h

Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

MODULE-3 LOW POWER CLOCK DISTRIBUTION 8 h

Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network.

MODULE-4 LOGIC SYNTHESIS FOR LOW POWER ESTIMATION TECHNIQUES 8 h

Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

MODULE-5 LOW POWER MEMORY DESIGN 8 h

Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

MODULE-6 LOW POWER MICROPROCESSOR DESIGN SYSTEM 8 h

Trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance

Text Book(s):

1. Low Power Design Methodologies-P. Rashinkar, Paterson and L. Singh, Kluwer Academic, 2002
2. Low power CMOS VLSI circuit design-Kaushik Roy, Sharat Prasad, John Wiley sons Inc.,2000.

Reference Book(s):

1. Low voltage CMOS VLSI Circuits-J.B.Kulo and J.H Lou, Wiley, 1999.
2. Low power digital CMOS design-A.P.Chandrasekaran and R.W.Broadersen, Kluwer,1995
3. Practical low power digital VLSI design-Gary Yeap, Kluwer, 1998.

21. COMMUNICATION NETWORKS

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
III	3	0	0	48	3	40	60	100

MODULE – 1 INTRODUCTION 8 h

Network Architecture- Layering and Protocols, Internet Architecture, Peer-to-peer network , Client/server network, Performance- Bandwidth and Latency, Delay × Bandwidth Product, High-Speed Networks, Application Performance Needs.

MODULE -2 CONNECTING NODES 8 h

Connecting links, Perspectives on Connecting, Encoding- NRZ, NRZI, Manchester, 4B/5B, Framing, Error detection, Reliable transmission, Ethernet and Multiple access networks, Wireless networks.

MODULE-3 QUEUING MODELS AND INTERNETWORKING 8 h

Queuing models : one or more servers, with infinite and finite queue size ,Infinite population
Internetworking: Switching and bridging, Basic Internetworking, IPv4, Addressing, Routing Protocols, Scale issues, Routers - Architecture, IPv6.

MODULE-4 END-TO-END PROTOCOLS 8 h

Simple Demultiplexer, Reliable Byte Stream, Remote Procedure Call, Transport for Real-Time Applications- Requirements, RTP Design, Control Protocol.

MODULE-5 CONGESTION CONTROL AND RESOURCE ALLOCATION 8 h

Issues in Resource Allocation, Queuing disciplines, TCP congestion control, Congestion Avoidance, QoS Applications: - Domain Name Resolution, File Transfer, Electronic Mail, WWW, Multimedia Applications.

MODULE-6 APPLICATIONS 8 h

Traditional Applications- SMTP, MIME, IMAP, HTTP, Web Services, Multimedia Applications- Session Control and Call Control, Resource Allocation for Multimedia Applications, Infrastructure Services- Name Service, Network management, Overlay Networks- Routing Overlays, Peer-to-Peer Networks, Content Distribution Networks.

Text Book(s):

1. Computer Networks-Larry L. Peterson, Bruce S, Devie, MK, 5th Edition
2. Telecommunication Network Design Algorithms-Aaron Kershenbaum, MGH, International Edition 1993.

Reference Book(s):

1. Communications Network Design and Analysis of Computer
Communication Networks-Vijay Ahuja, MGH, International Editions.
2. Internetworking with TCP/IP-Douglas E. Comer, Pearson Education, 6th Edition

22. GENETIC ALGORITHMS AND APPLICATIONS IN VLSI

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
III	3	0	0	48	3	40	60	100

MODULE 1 FUNDAMENTALS OF GENETIC ALGORITHM 8 h

Terminologies – Simple Genetic algorithms – steady state algorithm – Genetic operators-types of GA-Genetic algorithms vs. Conventional algorithms – GA example – GA for VLSI design, layout and test automation.

MODULE 2 PARTITIONING 8 h

Problem description – Circuit partitioning by genetic algorithms – hybrid genetic algorithms for ratio-cut partitioning.

MODULE 3 PLACEMENT AND ROUTING 8h

Placement: Standard cell placement – Macro cell placement – Standard cell placement on a network of workstations Routing: Steiner problem in graph – macro cell global routing

MODULE 4 GENETIC ALGORITHMS IN VLSI TESTING 9 h

Problem description – test generation frame work – test generation for test applications time reduction – deterministic/genetic test generators sequences-dynamic test sequence compaction – parallel algorithms for ATPG

MODULE 5 FPGA TECHNOLOGY MAPPING & PEAK POWER ESTIMATION 8 h

FPGA technology mapping: Circuit segmentation and FPGA mapping-circuit segmentation for Pseudo-Exhaustive testing. Peak power estimation: Problem description – application of GA – Estimation of peak single cycle and n-cycle powers-peak sustainable power estimation.

MODULE 6 APPLICATIONS OF GENETIC ALGORITHMS 8 h

Applications of Genetic based machine learning-Genetic Algorithm and parallel processors, composite laminates, constraint optimization, multilevel optimization, real life problem. - Standard cell placement - GA for ATG - GA vs Conventional Algorithm.

Text Book(s):

1. Genetic algorithms for VLSI design layout and test automation-Pinaki mazumder and Elizabeth M Rudnick,Pearson Edition, 2011.
2. Genetic algorithms in search, optimization and machine learning-David E Goldberg, Addison-Wesley, Longman Publishing Co., Inc. Boston, MA, USA, 2009.

Reference Book(S):

1. An introduction to Genetic Algorithm-Melanie Mitchell, PHI,New Delhi, Edition: 2004
2. Genetic algorithms in search, optimization and machine learning-David.E.Golberg, Addision-Wesley-1999
3. Neural Networks, Fuzzy logic and Genetic Algorithms, Synthesis and Applications-S.Rajasekaran and G.A Vijayalakshmi Pai, Prentice Hall of India, NewDelhi-2003
4. Genetic Programming: Automatic Discovery of Reusable Programs-John R.Koza, Forrest H.Bennett, David Andre, Morgan Kufmann, MIT Press, 1999.
5. Practical Genetic Algorithms-Randy L. Haupt, Sue Ellen Haupt, Second Edition, John Wiley & Sons, 2004

23. NANO ELECTRONICS

Semester	H / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
III	3	0	0	48	3	40	60	100

MODULE - 1 INTRODUCTION TO NANO ELECTRONICS 8 h

Top down Approach, the bottom up approach, why Nano electronics, Nanotechnology potential, the development of Microelectronics, The region of Nanostructures, The complexity Problem, The challenge initiated by Nano electronics.

MODULE - 2 MATERIALS FOR NANO ELECTRONICS 8 h

Semiconductors, Crystal structure and Crystal lattices: bonding in crystals, Electron energy bands, Semiconductor heterostructures, Lattice-matched and pseudomorphic heterostructure, Organic semiconductors, Carbon nanomaterials: nanotubes and fullerenes.

MODULE – 3 FABRICATION TECHNIQUES FOR NANOSTRUCTURES 8 h

Nano lithography, etching, physical and chemical deposition for fabrication of nanostructures and nanodevices; Techniques for characterization of nanostructures, Spontaneous formation and ordering of nanostructures; Clusters and nanocrystals, Methods of nanotube growth, Chemical and biological methods for nanoscale fabrication, Fabrication of nanoelectromechanical systems.

MODULE – 4 NANOELECTRONIC DEVICES 8 h

Resonant tunneling diodes, Field effect transistors, Single electron transfer devices, Potential effect transistors, Light emitting diodes and lasers; Nanoelectromechanical system devices, Quantum dot cellular automata.

MODULE – 5 NANO MEMORY DEVICES AND SENSORS 8 h

Nano ferroelectrics – Ferroelectric random access memory – Fe-RAM circuit design – ferroelectric thin film properties and integration – calorimetric sensors – electrochemical cells – surface and bulk acoustic devices – gas sensitive FETs – resistive semiconductor gas sensors –electronic noses – identification of hazardous solvents and gases – semiconductor sensor array.

MODULE – 6 SPINTRONICS 8 h

Introduction, Overview, History & Background, Generation of Spin Polarization Theories of spin Injection, spin relaxation and spin dephasing, Spintronic devices and applications, spin filters, spin diodes, spin transistors.

Text Book(s):

1. Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications-Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A.Stroscio, Cambridge University Press, 2012.
2. Fundamentals of Nanoelectronics-George W. Hanson, Prentice Hall, 2007.
3. Concepts in Spintronics – Sadamichi Maekawa.

Reference Book(s):

1. Introduction to Nanoelectronics-Mitin.V, Kochelap.V and Stroscio.M, Cambridge University Press, 2008.
2. Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum devices-Karl Goserl, Peter Glosekotter and Jan Dienstuhl, Springer, 2005.
3. Spin Electronics – David Awschalom

OPEN ELECTIVES

1. Business Analytics
2. Industrial Safety
3. Operations Research
4. Cost Management of Engineering Projects
5. Composite Materials
6. Waste to Energy

1. BUSINESS ANALYTICS

Semester	Hours / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
	3	0	0	48	3	40	60	100

MODULE – 1 BUSINESS ANALYTICS 8h

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modeling, sampling and estimation methods overview.

MODULE -2 TRENDINESS AND REGRESSION ANALYSIS 8h

Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology

MODULE -3 ORGANIZATION STRUCTURES OF BUSINESS ANALYTI 8h

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

MODULE -4 FORECASTING TECHNIQUES 8h

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

MODULE -5 DECISION ANALYSIS 8h

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

MODULE-6 RECENT TRENDS IN BUSINESS ANALYTICS 8h

Recent Trends in : Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism

Text Book(s):

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

2. INDUSTRIAL SAFETY

Semester	Hours / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
	3	0	0	48	3	40	60	100

MODULE – 1 INDUSTRIAL SAFETY 8h

Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

MODULE -2 FUNDAMENTALS OF MAINTENANCE ENGINEERING 8h

Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

MODULE-3 WEAR AND CORROSION AND THEIR PREVENTION 8h

Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

MODULE-4 FAULT TRACING 8h

Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

MODULE-5 PERIODIC AND PREVENTIVE MAINTENANCE 8h

Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance

MODULE-6 PROCEDURE FOR PERIODIC AND PREVENTIVE MAINTENANCE 8h

Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Text Book(s):

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.

Reference Book(s):

1. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
2. Foundation Engineering Handbok, Winterkorn, Hans, Chapman & Hall London

3. INDUSTRIAL SAFETY

Semester	Hours / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
	3	0	0	48	3	40	60	100

MODULE – 1 OPTIMIZATION TECHNIQUES 8h

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

MODULE -2 LINEAR PROGRAMMING 8h

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

MODULE -3 CLASSICAL OPTIMIZATION METHODS 8h

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

MODULE -4 SCHEDULING AND SEQUENCING 8h

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

MODULE -5 GAMES THEORY 8h

Competitive Models,Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

MODULE-6 EVOLUTIONARY ALGORITHMS 8h

An overview of evolutionary algorithms, Simulated annealing algorithm, Genetic algorithm, Particle swarm optimization

Text Book(s):

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008

Reference Book(s):

1. Hitler Libermann Operations Research: McGraw Hill Pub. 2009
2. Pannerselvam, Operations Research: Prentice Hall of India 2010
3. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

4. COST MANAGEMENT OF ENGINEERING PROJECTS

Semester	Hours / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
	3	0	0	48	3	40	60	100

MODULE – 1 INTRODUCTION 8h

Introduction and Overview of the Strategic Cost Management Process

MODULE -2 COST CONCEPTS 8h

Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

MODULE -3 PROJECT MANAGEMENT 8h

Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

MODULE -4 COST BEHAVIOR 8h

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis.

MODULE -5 PRICING STRATEGIES 8h

Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

MODULE-6 QUANTITATIVE TECHNIQUES 8h

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory

Text Book(s):

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting

Reference Book(s):

1. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
2. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd

5. COMPOSITE MATERIALS

Semester	Hours / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
	3	0	0	48	3	40	60	100

MODULE 1 INTRODUCTION 8h

Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance

MODULE 2 REINFORCEMENTS 8h

Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

MODULE 3 MANUFACTURING OF METAL MATRIX COMPOSITES 8h

Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications..

MODULE 4 MANUFACTURING OF POLYMER MATRIX COMPOSITES 8h

Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

MODULE 5 STRENGTH OF COMPOSITE MATERIALS 8h

Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

MODULE 6 METAL MATRIX COMPOSITES 8h

Characteristics of MMC, various types of metal matrix composites alloy vs. MMC, advantages of MMC, limitations of MMC, Reinforcements – particles – fibres. Effect of reinforcement - volume fraction – rule of mixtures. Processing of MMC – powder metallurgy process - diffusion bonding– stir casting – squeeze casting, a spray process, Liquid infiltration In-situ reactions-Interface measurement of interface properties- applications of MMC in aerospace, automotive industries

Text Book(s):

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007. 5th Edition, New Delhi, 2015.

Reference Book(s):

1. Hand Book of Composite Materials-ed-Lubin.
2. Composite Materials – K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L. Chung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi

6. WASTE TO ENERGY

Semester	Hours / Week			Total	Credit	Max Marks		
	L	T	P	**hrs**	C	CIE	SEE	TOTAL
	3	0	0	48	3	40	60	100

MODULE – 1 INTRODUCTION TO ENERGY FROM WASTE 8h

Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

MODULE – 2 WASTE TO ENERGY OPTIONS 8h

Waste to energy options: combustion (unprocessed and processed fuel), gasification, aerobic digestion, anaerobic digestion, fermentation

MODULE – 3 BIOMASS PYROLYSIS 8h

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications..

MODULE – 4 BIOMASS GASIFICATION 8h

Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation

MODULE – 5 BIOMASS COMBUSTION 8h

Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

MODULE – 6 BIOGAS 8h

Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Text Book(s):

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.

Reference Book(s):

1. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
2. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.